Overview
As the world’s population continues to embrace the digital revolution and finds new ways to make use of the available bandwidth, understanding how the network is performing becomes a critical task within network management. Analytics / assurance (assessing and improving network performance) and monitoring (protection of national and corporate security) are as important as bandwidth utilization / efficiency.

Stakeholder organisations such as commercial network operators and government intelligence agencies monitor, analyze & intercept network traffic to carry out these tasks. This in turn requires solution providers to deliver reliable, flexible & cost effective products that capture every frame or packet on the wire.

These products must adapt to changing and improving threats and therefore cannot rely on commercially available, fixed-function, off-the-shelf silicon. Adaptable FPGA technology is the perfect fit.

Aliathon in partnership with Nallatech, can offer a feature rich and easy to use platform to help our network analytics / assurance clients develop products to meet these challenges.

Our solution allows fine-grained access to any part of the incoming data structure thereby allowing upstream analysis of the frame overhead, packet headers, raw client signals and associated stats.

Functional Block Diagram

Detailed Feature Set

**OTN**
- OTU2/1e/2e/2f/1f, OTU1.
- 3-stage demuxing (ODU2/1/0).
- GFP, GMP, AMP, BMP deframing & de-mapping.
- GFEC, G.975.1 eFEC.

**SONET/SDH**
- Support for HO & LO Channelized paths.
- Support for PoS, GFP, ATM, HDLC
- E1/T1 Deframing.

**Upstream Processing**
- Delivered via PCIe (GEN2 / GEN3 ).
- Access to raw TDM or packetized data.
- Host Interface to facilitate WinPcap drivers/libraries.

**Ethernet**
- 1Gb/10Gb
FPGA Architecture (per port)
FPGA Architecture Overview

The design can be configured to have as many universal probe line interfaces (UPLI’s) as is required for the application and/or can be supported by the target FPGA. Each UPLI feeds to the memory management unit which is configured to buffer the data in the granularity required by the upstream system.

Each UPLI is individually configured with the protocol mappings of choice as is shown in the diagram opposite.

The host interface core delivers the raw data + line health info to the upstream processing unit. The defects/errors/stats registers and data memory locations are read by the upstream processing unit over PCIe or an unused optical port.

Each client is deframed and demapped in accordance with the relevant standard irrespective of its rate relationship with the transport container (constant bit rate or asynchronous signals requiring transmission convergence). Demapping techniques employed are the asynchronous mapping procedure (AMP), bit-synchronous mapping procedure (BMP) and generic mapping procedure (GMP).

Client signal types and their mapping options are shown below.

Statistics, errors and defects are provided for all protocols and all layers of the design via Aliathon’s configurable micro-processor link that can be altered to suit any standard or proprietary bus format.

10G Datapath Options

SONET/SDH

- Native OC192/STM64 (or proprietary SDH structure).
- OC192/STM64 -> 10GbE (WANPHY Ethernet transport).
- OC192/STM64 -> PoS -> Packet (legacy packet transport).
- OC192/STM64 -> GFP-Packet (modern packet transport).

Ethernet

- Native 10GbE (LANPHY).

OTN

- Native OTU2/2e/1e (or proprietary OTU2k structure).
- OTU2 -> OC192/STM64 (legacy TDM transport).
- OTU2 -> OC192/STM64 -> 10GbE (SDH packet transport extender).
- OTU2e/1e -> 10GbE (modern Ethernet transport).

<10G Configurations

The solution can be configured to support subrate (<10Gb) client. Client signal options can be as follows:

- OTN OTU1 (carrying subrate OTN, SONET/SDH or packet).
- SONET/SDH OC3/STM1, OC12/STM4 or OC48/STM16 (carrying subrate SONET/SDH, PDH or packet).
- Ethernet (10/100/1000).

Software Domain

To facilitate upstream processing of the raw TDM payloads and/or packet structures a host interface block has been created to be compliant with WinPcap. Using WinPcap’s open standard drivers and libraries means that our clients can easily integrate this solution with their own software environment or use open source network tools such as WireShark, Nmap or Snort.
Target Hardware Platforms

**Nallatech PCIe-287N 7-Series FPGA Network Processing Card**
- Full-height, 3/4-length PCIe Gen2.
- 4 x SFP+ Ports.
- Dual Xilinx Kintex-7 K325T FPGAs.
- 6 x banks of 9MB QDRI-II SRAM
- 2 x banks of 1GB DR SDRAM.

**Nallatech PCIe-395n Altera Stratix V FPGA Computing Card**
- Full-height, 3/4-length PCIe Gen3.
- 4 x SFP+ Ports.
- Single Altera Stratix-V A7 or D8.
- 4 x banks of DDR3 SDRAM, up to 32GB.

**Nallatech PCIe-385n Altera Stratix V FPGA Computing Card**
- Half-height half-length PCIe Gen3.
- 2 x SFP+ Ports.
- Single Altera Stratix-V A7 or D5.
- 2 x banks of DDR3 up to 16GB.

Integrated Servers and Blades

Each of the FPGA cards above are available pre-integrated in server and blade platforms from leading vendors such as IBM (iOEM program) and HP (3PO program).  [Click here](#) to read more.

Contact Us

- info@aliathon.com
- +44 (0)1383 737 736
- www.aliathon.com

Aliathon Ltd
Evans Business Center,
Pitreavie Court
Dunfermline, Fife, KY11 8UU
Scotland, UK